IN THE ABSTRACT:

This new abstract will replace the prior abstract in the application:

Abstract

A digital system is provided having at least one processor with an associated multi-segment local memory circuit. Validity circuitry is operable to indicate if each segment of the plurality of segments holds valid data. Dirty bit circuitry indicates if data within the local memory is incoherent with a secondary memory. DMA circuitry can transfer blocks of data/instructions between the local memory and the secondary memory. The valid bits and dirty bits are set in response to DMA transfers. In a first mode, the DMA circuitry transfers an entire block from the local memory to the secondary memory; in a second mode, the DMA circuitry transfers only segments marked as being dirty. Transaction requests by the processor to locations within the local memory are stalled if the requested segment has not yet been loaded by a DMA transfer.